WHAT WE CLAIM IS:

1. A semiconductor integrated circuit device comprising:

a first low noise amplifier into which a reception signal of a first frequency band is to be inputted;

a second low noise amplifier into which a reception signal of a second frequency band is to be inputted, the second frequency band being higher than the first frequency band;

a first ground pin electrically connected to said first low noise amplifier; and

a second ground pin electrically connected to said second low noise amplifier,

wherein said first low noise amplifier and said second low noise amplifier are monolithically integrated on one semiconductor chip, and

wherein a distance between said first ground pin and a nearest corner of four corners of said semiconductor chip to said first ground pin is shorter than a distance between said second ground pin and a nearest corner of four corners of said semiconductor chip to said second ground pin.

2. The semiconductor integrated circuit device according to claim 1, wherein said first ground pin and said second ground pin are disposed on a single side of said semiconductor chip.

3. The semiconductor integrated circuit device according to claim 1, further comprising:

a first input pin electrically connected to said first low noise amplifier; and

a second input pin electrically connected to said second low noise amplifier,

wherein a reception signal of said first frequency band is to be applied to said first input pin and a reception signal of said second frequency band is to be applied to said second input pin.

4. The semiconductor integrated circuit device according to claim 3,

wherein said first input pin and said second input pin are disposed on a single side of said semiconductor chip.

5. The semiconductor integrated circuit device according to claim 4,

wherein said first and second input pins and said first and second ground pins are disposed on a same side of said semiconductor chip.

6. The semiconductor integrated circuit device according to claim 1, further comprising:

a first receiving mixer into which a local oscillation signal of said first frequency band is to be inputted; and

a second receiving mixer into which a local oscillation

signal of said second frequency band is to be inputted,

wherein said first receiving mixer and said second receiving mixer are further monolithically integrated on said one semiconductor chip together with said first low noise amplifier and said second low noise amplifier.

7. The semiconductor integrated circuit device according to claim 1,

wherein a circuit corresponding to one of said first low noise amplifier and said second low noise amplifier is provided at a location such that a distance from a pin end projecting to outside a package to a pad connected to said one of said first low noise amplifier and said second low noise amplifier is the shortest in comparison with distances from ends of other lead pins to pads corresponding thereto.

8. The semiconductor integrated circuit device according to claim 1, further comprising:

a first bias circuit electrically connected to said first low noise amplifier; and

a second bias circuit electrically connected to said second low noise amplifier,

wherein each of said first bias circuit and said second bias circuit is electrically connected to another ground pin, different from that of said first ground pin and said second ground pin.

9. The semiconductor integrated circuit device according to claim 1, further comprising:

a first output pin electrically connected to said first low noise amplifier; and

a second output pin electrically connected to said second low noise amplifier,

wherein a reception signal of said first frequency band amplified through said first low noise amplifier is outputted from said first output pin and a reception signal of said second frequency band amplified through said second low noise amplifier is outputted from said second output pin.

10. The semiconductor integrated circuit device according to claim 1, further comprising:

a first input pin electrically connected to said first low noise amplifier;

a second input pin electrically connected to said second low noise amplifier,

a first output pin electrically connected to said first low noise amplifier; and

a second output pin electrically connected to said second low noise amplifier,

wherein a reception signal of said first frequency band is to be applied to said first input pin and a reception signal of said second frequency band is to be applied to said second input pin, and

wherein a reception signal of said first frequency

band amplified through said first low noise amplifier is outputted from said first output pin and a reception signal of said second frequency band amplified through said second low noise amplifier is outputted from said second output pin.

11. The semiconductor integrated circuit device according to claim 10,

wherein said first low noise amplifier comprises a first bipolar transistor having an emitter electrically connected to said first ground pin, a base electrically connected to said first input pin, and a collector electrically connected to said first output pin, and

wherein said second low noise amplifier comprises a second bipolar transistor having an emitter electrically connected to said second ground pin, a base electrically connected to said second input pin, and a collector electrically connected to said second output pin.

12. The semiconductor integrated circuit device according to claim 1,

wherein said first low noise amplifier and said second low noise amplifier include a first bipolar transistor and a second bipolar transistor, respectively, and

wherein a distance between a pad to which an emitter of said bipolar transistor of either said first low noise

amplifier or said second low noise amplifier is connected and an end of a pin corresponding thereto is the shortest.

13. The semiconductor integrated circuit device according to claim 1,

wherein said first ground pin and said second ground pin are disposed so as not to be adjacent to each other.

14. The semiconductor integrated circuit device according to claim 13, further comprising:

a first input pin electrically connected to said first low noise amplifier;

a second input pin electrically connected to said second low noise amplifier,

a first output pin electrically connected to said first low noise amplifier; and

a second output pin electrically connected to said second low noise amplifier,

wherein a reception signal of said first frequency band is to be applied to said first input pin and a reception signal of said second frequency band is to be applied to said second input pin, and

wherein a reception signal of said first frequency band amplified through said first low noise amplifier is outputted from said first output pin and a reception signal of said second frequency band amplified through said second low noise amplifier is outputted from said second output

pin.

15. The semiconductor integrated circuit device according to claim 14,

wherein said first low noise amplifier comprises a first bipolar transistor having an emitter electrically connected to said first ground pin, a base electrically connected to said first input pin, and a collector electrically connected to said first output pin, and

wherein said second low noise amplifier comprises a second bipolar transistor having an emitter electrically connected to said second ground pin, a base electrically connected to said second input pin, and a collector electrically connected to said second output pin.

16. The semiconductor integrated circuit device according to claim 1, wherein each of said first and second low noise amplifiers is further electrically connected to an input pin and an output pin, any of said first and second ground pins being provided between said input pin and said output pin.

17. The semiconductor integrated circuit device according to claim 16,

wherein each of said first and second low noise amplifiers includes a bipolar transistor having an emitter electrically connected to one of said first and second

ground pins, a base electrically connected to said input pin, and a collector electrically connected to said output pin.